Lab4: Brandon Kowal, Bernard Owusu Sefah

Parity Generator and Checker

Abstract

The even Parity generator had a 2-bit message when the truth table is made it can be shown how if there was an odd number of 1 input it would output another 1 to make it even output. The even Parity checker has a 3-bit message. The 3rd input to this one is from the parity generator, so if the generator is working correctly than the checker will not give a 1 output.

Introduction

This Lab is to learn the two-level combinational logic circuit prototyping. So, the lab will have us design and test a parity generator circuit that generates and even parity bit for a binary message and design a parity checker.

Methods

1.Developed a simple parity generator using the 7404, 7400 and the 7404 IC’s.

2. Connect each pin to the corresponding ground and Vcc to the ETS-7000 to each IC.

3. Connect the parity generator to SW1 and SW2 to the ETS-7000 then connect the output of the parity generator to any led output.

4. Power up the ETS-7000 and then compare the output to the truth table.

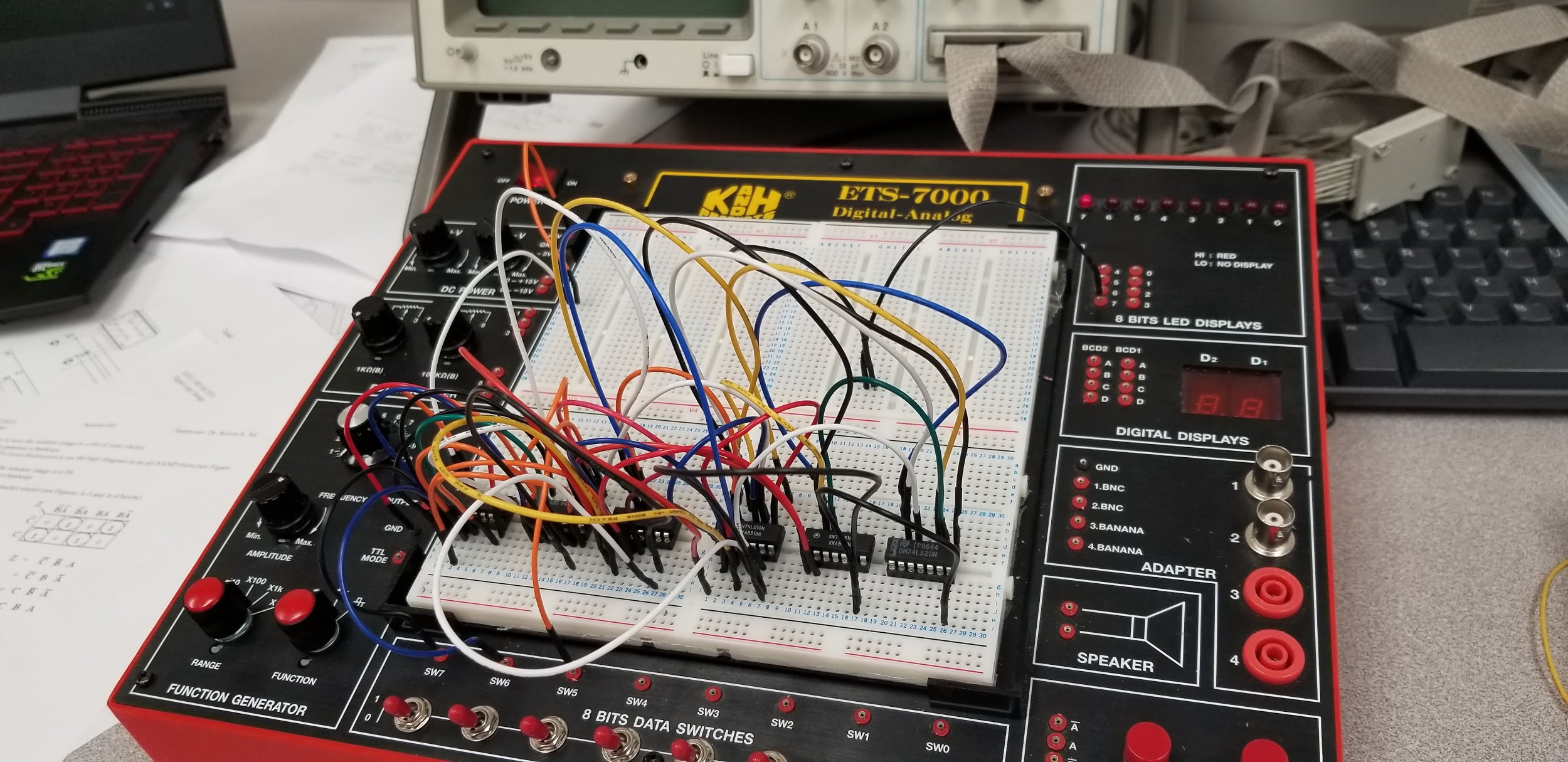
5. Use the 7404, 7410, 7420 to develop a parity check and then connect the parity checker to the parity generator without changing anything on the parity generator.

6. Power on the ETS-7000 and test the output with the truth table.

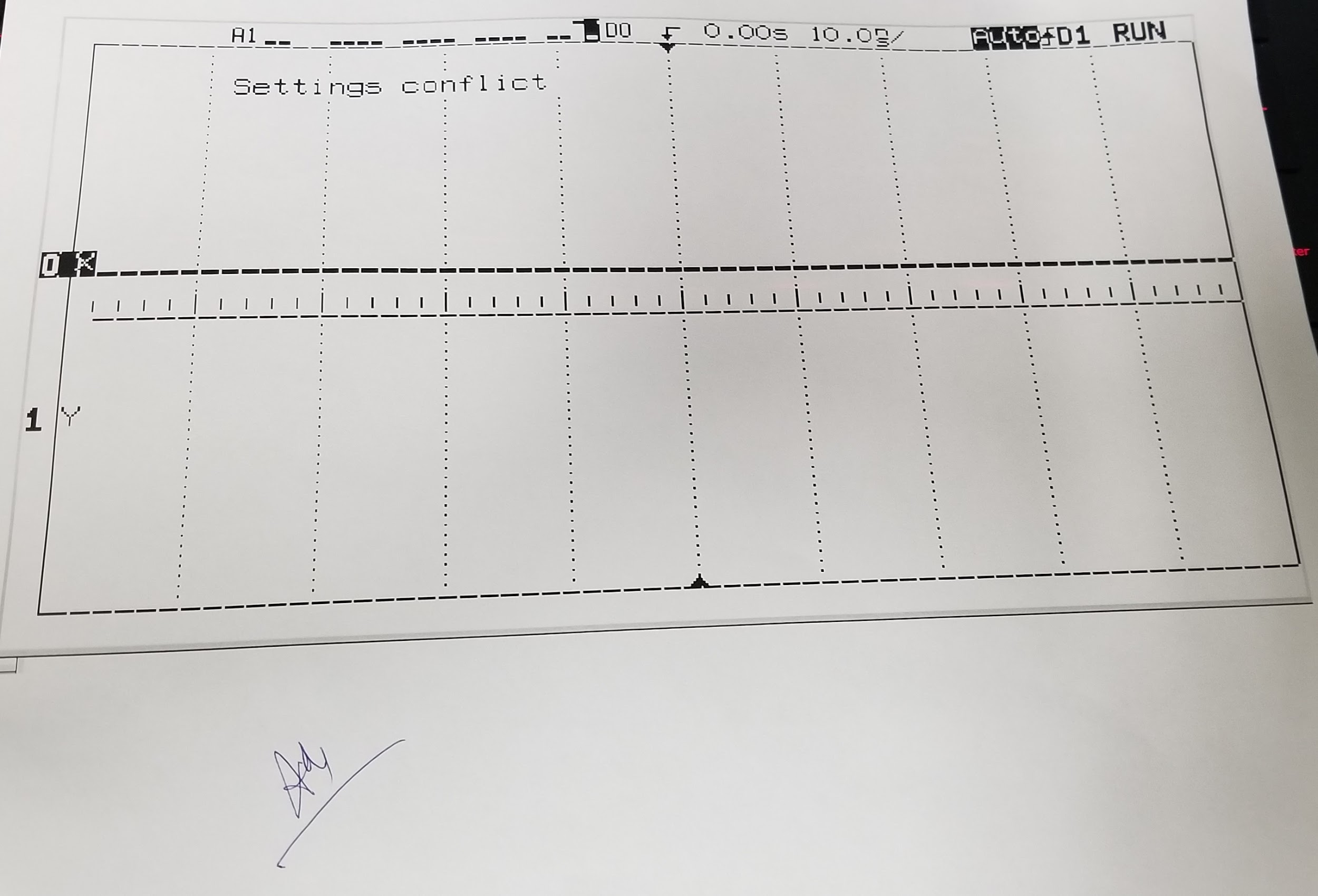
7. Connect the parity generator and checker to the MSO and induce a 1bit error to the 3 bit and capture the results from the MSO.

Results

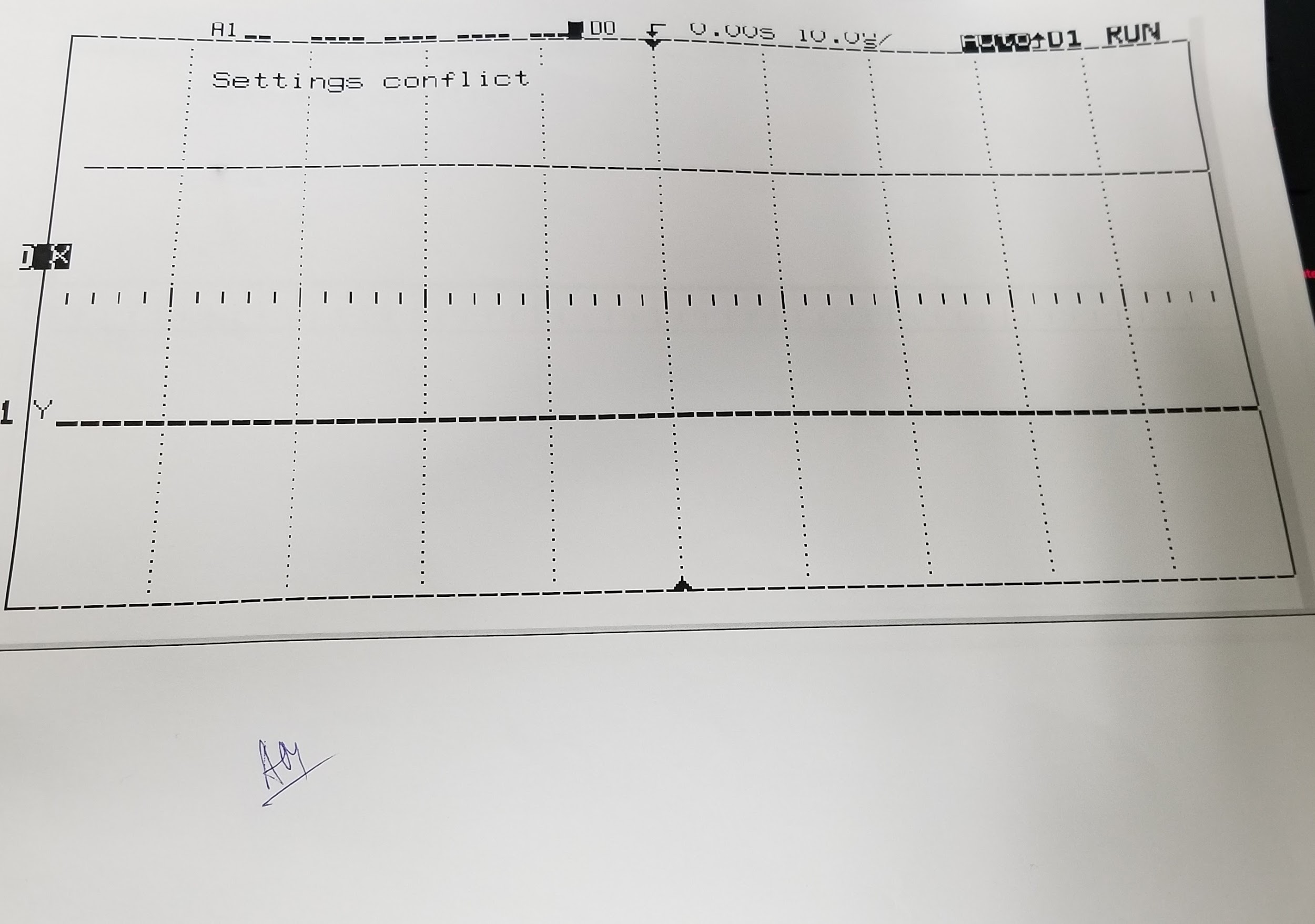
Parity Generator and Parity Check



Before Inducing 1bit error



After Inducing 1bit error



Discussion

We wired our parity generator we created from the prelab in the lab. During the lab we run into some issues connecting the parity generator to the parity checker because some of our inputs and outputs were connected in the wrong pins. We had disconnected our parity generator and start over again from scratch and troubleshoot what the problem was. We discovered that the parity checker was wired wrong, so we had developed a new parity checker and then connect it to the parity generator.

Conclusion

In this lab we were able to design a parity generator and a parity checker. The generator gave a correct output based on our inputs and with the checker it only again when there was an odd input when they were together only 0 outputs were given and that’s what the even generator and checker is supposed to do.

Appendix

Lab Attendance: Bernard Owusu Sefah: Yes Brandon Kowal: Yes

Involvement in Lab: Bernard Owusu Sefah: 55 Brandon Kowal: 45

Involvement in Lab Report: Bernard Owusu Sefah: 50 Brandon Kowal: 50